

A MTCA.4 Clock and Control System for the EuXFEL 2-D Detectors: Tests and Further Development

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Abstract– This paper presents the experiences with the clock and control (CC) system for the EuXFEL mega-pixel detectors. The CC system is the combination of an MTCA.4 based AMC and a Rear Transition Module (RTM), which resides in a MTCA.4 crate with the Timing Receiver (TR) board and the crate CPU unit. The main function is to synchronise the DAQ system to the general EuXFEL timing. The firmware for the CC system which runs on a Xilinx Virtex5 FPGA on the AMC board is described in detail. Additionally, the tests that have performed to validate the functionality of the CC system are presented along with the resulting modifications for the final version of the hardware.

I. INTRODUCTION

The design and the development of the hardware for the Clock and Control (CC) system for the European Free Electron Laser (EuXFEL) megapixel detectors is described in [1]. The system is based on a combination of a general purpose MTCA.4 AMC board and a compatible Rear Transition Module. A DESY designed AMC board [2] having a Xilinx V5LX50T FPGA provides processing power and connectivity for different subsystems in the EuXFEL. The RTM is a custom designed PCB that is connected to the AMC via the 60-pin ADF connector which provides up to 54 differential links in addition to the power and the control signals for the MTCA.4 operation. The RTM in turn provides the connectivity to the Front End Electronics (FEE) units at the detector end through the use of a stacked RJ45 connector. Fig. 1 shows the CC RTM prototype.

The structure of the EuXFEL 2D detector readout system for the LPD detector can be seen in Fig. 2, where the CC system sits in a MTCA.4 crate along with the timing receiver (TR) board and the crate CPU. The timing receiver board is responsible for the synchronisation of the detectors and the DAQ system to the general EuXFEL timing.

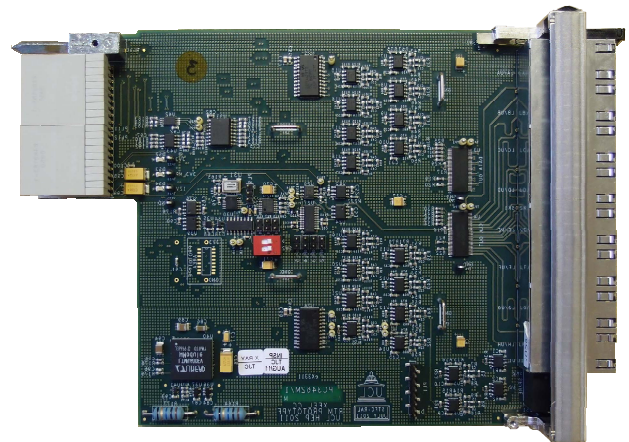


Fig. 1. The CC RTM prototype.

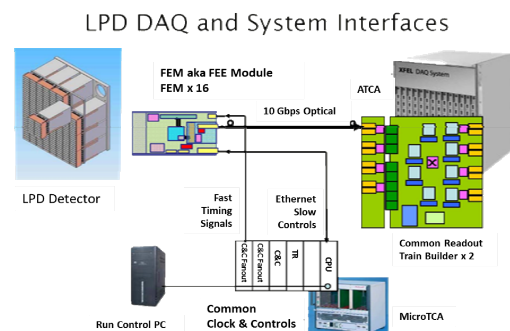


Fig. 2. The structure of the EuXFEL 2D detector readout system.

The EuXFEL facility will generate coherent and intense X-ray flashes with a ~ 4.5 MHz bunch frequency [3]. The Timing Receiver (TR) board [4], housed in the same crate as the CC system delivers the bunch clock which is the same frequency as the bunch frequency or double that frequency at ~ 9 MHz to the CC through the MTCA.4 backplane on TCLK1 line [9]. In addition to the bunch clock, there are backplane MLVDS links to the TR. These links include the Start/Trigger signal which denotes the start of the bunch train, the telegram data that carries the information comprising the current bunch train ID and the bunch pattern index, and the 108 MHz telegram clock to which the telegram data is sent synchronously. Additionally, extra connections also exist on the bussed

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MLVDS links for various functions such as resetting the CC system and status from the CC system.

At the detector end there are FEE units which transport the detector data to the train builder (TB) which in turn sends its data to the PC farm [5]. The CC system multiplies the bunch clock received from the TR to 99 MHz and distributes this clock to the FEE units in order to synchronise the DAQ system to the EuXFEL facility timing.

The clocking circuitry (Fig. 3) on the RTM includes a local crystal oscillator, PLL and non-PLL based multiplexers in order to provide an uninterrupted, stable clock to the final PLL which multiplies the bunch clock to provide the 99 MHz clock. This clock is then converted to differential and goes into a 1:16 LVDS fan-out chip. A copy of this clock also goes back to the FPGA through the RTM connector.

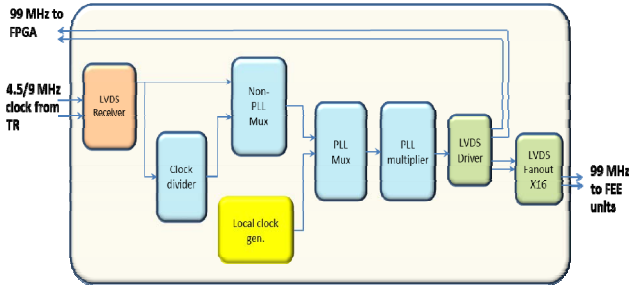


Fig. 3. Block diagram of the clocking circuitry on the CC RTM

The link between a FEE unit and the CC system consists of 4 LVDS pairs which fit into a single RJ45 connector. In addition to the 99 MHz clock, control data and the VETO information are sent to the FEE units. The control data which is called the FAST data contains synchronising information such as the start and the end of a bunch trains along with the train ID numbers and the bunch pattern index values. The status information from the FEE units is received on the remaining differential link. By using a 2x8 RJ45 connector up to 16 FEMs which make up a 1 megapixel detector can be supported. The use of CC slaves provides the scalability of the system to support up to 6 megapixel detectors in a single 12 slot MTCA.4 crate as shown in Fig. 4. The CC slaves get the 99 MHz clock from the master on the MTCA.4 backplane on the TCLK2 line.

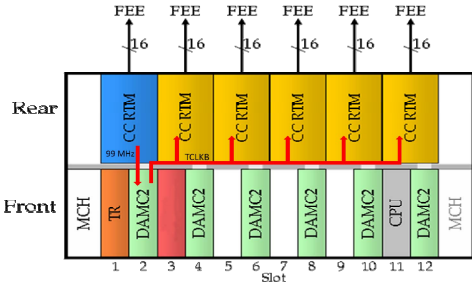


Fig. 3. The CC master (blue) and the slave (yellow) boards along with the TR board on a 12-slot MTCA.4 crate

II. THE FPGA FIRMWARE

The FPGA firmware for the CC system is built around a bus/register structure called the II Bus [6], whose registers are accessed through either the PCIe link to the crate processor or

the functional blocks attached to the bus as shown in Fig. 5. The EuXFEL central software system controls the CC system through the PCIe link.

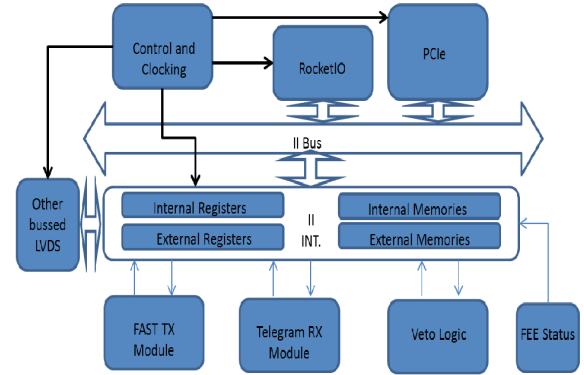


Fig. 5. The block diagram of the CC FPGA firmware

The FAST TX module generates the control messages to the FEE units (FAST data) that are sent synchronously to the 99 MHz clock. The protocol for the messages can be seen in table I. The values for the payload are read from the II Bus registers.

TABLE I. THE PROTOCOL FOR THE FAST DATA

Command	Start Bits	Payload	Purpose
START	1100	Train ID (32 bits) + Bunch Pattern Index (8 bits) + Checksum (8 bits)	Notifies FEE of coming train
STOP	1010	None	Notifies FEE that the train ended
RESET	1001	None	Reset FEE
Reserved	1111		

The telegram RX module receives the telegram data from the TR board on the same crate in order to extract the train ID numbers and the bunch pattern index values from the serial data received synchronously to a 130 MHz telegram clock. These values are written to the respective registers on the II Bus.

The veto system for the 2D detectors takes the information from the veto sources and sends commands to the FEEs in order to skip the detector data related to certain bunches, thus saving storage in the detector ASICs [7]. The veto sources can be avalanche photo diodes, machine protection system and so on. Between the veto sources and the FEEs there are two functional entities, namely the veto units and the veto sources.

The veto logic module in the CC firmware can act as both the veto unit and the user or just the veto user. The function of a veto unit is to gather the data coming from the possible veto sources and make decisions on which bunch data is to be rejected. The veto unit receives the data from the veto sources through 2.5 Gbps high speed serial optical links with a low overhead higher level protocol. The data incorporating the veto decisions are sent to the veto users on the identical physical layer with a different high level protocol.

The veto user processes the information from the veto unit and formats this data to be sent synchronously to the 99 MHz clock to the FEE units. This protocol is shown in Table II.

The veto unit for the 2D detectors is envisaged as a separate MTCA.4 board [7]. However, until the hardware for this unit is developed, the CC system will act as both the veto unit and the veto user. Either acting solely as a veto user or both the veto unit and the user, the CC system will make use of the high speed RocketIO links on the FPGA and the SFP modules that can be attached to the DAMC2. The II Bus registers provide the link between the veto logic and the RocketIO block.

In addition to the modules shown in Fig. 5, further test related modules can be attached to the II Bus such as the PRBS generator block which can be used to test the data link.

TABLE II. THE PROTOCOL FOR THE CC FEE VETO LINK

Command	Start Bits	Payload	Purpose
VETO	110	Bunch ID (12 bits) + 0000	Identifies bunch ID to be vetoed
NO VETO	101	Bunch ID (12 bits) + 0000	No veto defined for that bunch ID
GOLDEN	111	Bunch ID (12 bits) + 0000	Identifies bunch as golden
Reserved	100	Bunch ID (12 bits) + 0000	

III. TESTS WITH THE SYSTEM

A. Initial Tests

The first tests with the CC RTM involved ensuring the correct power-on when coupled with the DAMC2 in a MTCA.4 crate. The AMC board turns the 12 V power for the RTM on when the FRU record for the RTM is checked by the MCU and access to the I2C extender is established in order to read the status signals according to the MTCA.4 standard. The MCU then enables the DC-DC converter on the RTM in order to generate the power for the 3.3V voltage rail. The power-on tests for the first manufactured RTM initially failed. After correcting the values for the timeout capacitors for the hot-swap voltage controller on the DAMC2 the management power turned on. The last problem involved faulty soldering of the DC-DC converter on the RTM on the first prototype board tested. The DC-DC converter on this board was removed allowing other tests which will be presented next. The other prototype boards did not show this problem.

After the initial tests the operation of the clock circuitry was tested. There are two ways of generating the 99 MHz FEE clock. The first involves the local oscillator generating 9 MHz and the final PLL multiplying it. The second is to get the 9 MHz or 4.5 MHz clock from the TR board through the TCLK1 line on the MTCA.4 backplane. Verifying the operation of the clock circuitry also tests the RTM connection to the FPGA on DAMC2. As a result of the tests the 99 MHz clock was generated successfully from both the clock sources without any problems.

B. Clock Jitter

One of the most important performance metrics for the CC system is the jitter on the 99 MHz FEE clock. This clock is the only clock that provides the synchronisation of the FEE units with the main EuXFEL facility timing. The initial jitter specification is to have a Time Interval Error (TIE) below 200 ps for this clock. The jitter was measured using an Agilent

MSCO scope with the Agilent supplied jitter analysis software EZJIT. The test points on the PCB are on the first output of the 1:16 LVDS fan-out chip just before the RJ45 connector.



Fig. 6: The scope snapshot showing the TIE on the 99MHz clock

The current configuration of the CC RTM showed a high TIE and period jitter reading on the 99 MHz clock with the shape of the histogram suggesting a high amount of deterministic jitter. Fig. 6 shows the TIE snapshot from the scope. The scope screen is divided into three parts where the top part shows the clock waveform, the middle shows the histogram and the bottom part shows the spectrum of the jitter with the frequency on the horizontal axis and the jitter value on the vertical. Additionally, in the very bottom of the screen statistics for the jitter histogram can be seen. There is a high peak around the 780 KHz and a smaller peak at double this frequency. This corresponds to the switching frequency of the DC/DC converter, LTM4600EV, set on the CC RTM. Therefore, we can infer that the main jitter contribution comes from the ripple on the 3.3 V output from the DC/DC converter.



Fig. 7. The TIE snapshot corresponding to the case where 3.3V power is supplied externally.

Another test involved the RTM board with the DC/DC converter removed. We provided the 3.3V from an external power supply with cables soldered on to each side of the output bulk capacitor of the removed DC/DC converter. The resulting TIE measurements (Fig. 7) showed much improved

values, with the jitter histogram suggesting the jitter in the system is mostly random.

The further tests involved applying filtering on the 3.3 V rail to reduce the jitter readings. LTM4600EV was soldered on a small PCB and this PCB was attached to the CC RTM. Fig. 8 shows the most promising jitter readings which were obtained when a LC filter (1uH/1UF) is attached to the output of the DC/DC converter in addition to the required capacitors.

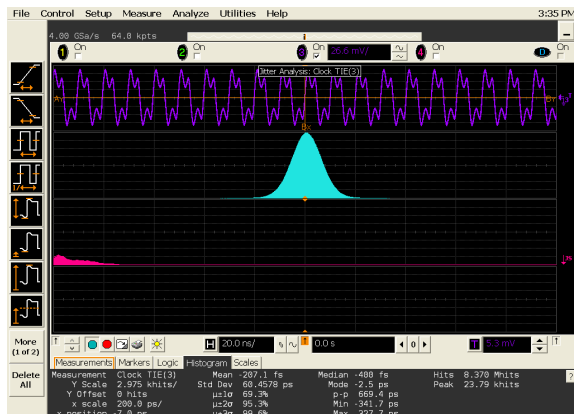


Fig. 8. The TIE snapshot corresponding to the case where the DC converter's output is filtered.

We envisage further improvements when this filtering scheme is employed on the final version of the CC RTM and the voltage plane for the clocking circuitry is separated from the main power plane by a ferrite bead.

C. Cable Length

Another important issue is the reliable data and clock transmission over long cables in the absence of a DC balanced data. The space limitations in the experimental area necessitate long cable lengths.

The clock and the data links to the FEE units are all AC coupled. Because the data sent to the FEEs is not DC balanced, a special circuitry on the receiver side is used to alleviate the DC wander [8]. As shown in Fig. 9 this circuitry uses a feedback to hold the signal level beyond the RC constant. By having two LVDS buffers in series it limits the data rate and the maximum cable length to be used for the FAST data link.

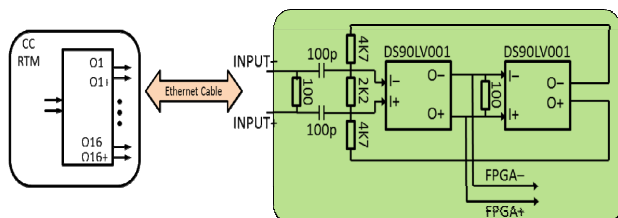


Fig. 9. The receiver circuitry for the AC coupled links on the FEE side

The tests involved using a data pattern which would cause a high DC wander on the AC coupled data link. The data is generated such that short bursts of 22-bit Pseudo Random Bit Sequence (PRBS) words are interspersed between long sequences ones or zeros. The sequence always starts with a

predefined start word for synchronisation. The data is sent in a source-synchronous way to the 99 MHz FEE clock. Fig. 10 presents a scope output showing the clock and the bursts of data.

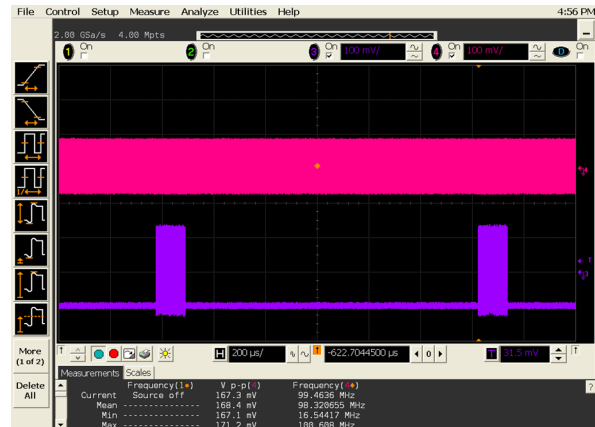


Fig. 10. Scope snapshot showing the PRBS words interspersed with long periods of zero.



Fig. 11. Experiment setup involving the prototype LPD FEM board

For the receiving circuitry a prototype FEE board designed for the LPD detector was used [10]. Fig.11 shows the FEM board connected to the CC system. Both the clock and the data channels on the receiver side had the special feedback circuitry which also has a RJ45 connector and 100 ohm balanced, length-matched LVDS lines going straight into the FPGA on the FEE board. The receiving circuitry transfers the data to the FPGA on the receiver card and the data is compared to the data generated on the receiver card in tandem. In the receiver firmware there is a word and a bit error counter to observe the error rate. The Chipscope analysis software running on the receiver provides the ability to view the data transmission and the error rate.

The tests were performed using Ethernet cables of lengths 10 m, 15 m, 20 m, 30 m and 50 m. There were no errors observed during a running period of more than 24 hours with the CAT6 SFTP cables up to 30m. Fig. 12 presents a Chipscope snapshot from the test with a 30m CAT6 SFTP cable showing correctly received random data after a long period of zero data. The random data test failed at the 50 m cable. The data word denoting the start of the random sequence was not properly captured every time due to the reduced voltage swing at the end of the cable. If there is a need to support a 50m cable length, MLVDS drivers have to be tested for data and clock transmission.

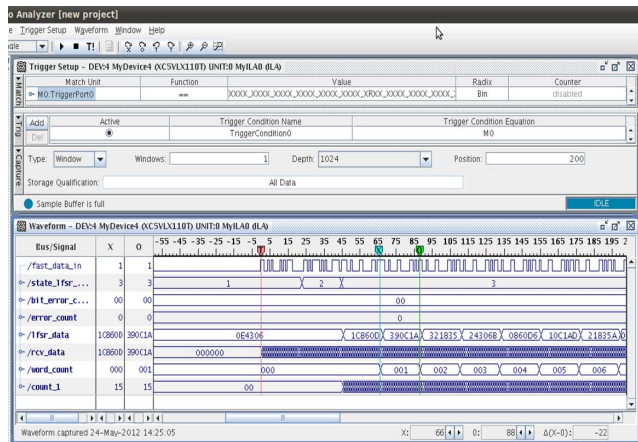


Fig. 12. A Chipscope snapshot from the long cable tests

IV. CONCLUSIONS

The experience with the first prototype of the CC system has been positive. The performance tests showed that there is a need for improvement especially the jitter readings on the 99 MHz line. Further tests to reduce the jitter value on this clock tell us that this is achievable with the solution of applying a filter at the output of the DC/DC converter and the power plane for the clocking circuitry being separated from the main power plane by a ferrite bead. The required length of the cable between the CC system and the FEE units is not finalised yet, however the system can support up to a 30m cable with the current configuration, albeit in the lab conditions. Further work on improving this performance metric is being undertaken. Additionally, the tests involving the actual FEE hardware and a prototype DAQ system integration test are being done.

The CC hardware/firmware system is designed to provide the flexibility, extensibility and scalability to support possible future upgrades to the 2D megapixel detectors. The final version of the CC hardware is currently being designed and will be manufactured early 2013.

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